Development and Characterization of an NMOS based Half-Adder Digital Logic Circuit using a Four-Mask Process

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Abstract - In this work, we present a comprehensive study on the design, fabrication and electrical characterization of an NMOS based half adder, created using only 200u x 10u MOSFETs. The four-mask fabrication process used in the lab incorporated thermal oxidation, phosphorus diffusion, photolithography, HF etching, and aluminum metallization and lift-off processes to simultaneously create 6 die per sample, each of which includes the half-adder and a variety of related subcircuits, including 4 test MOSFETs, TLM testing pads, an inverter, NAND gate, and NOR gate . The design of the half adder was primarily made out of NAND gates. The electrical testing showed that the individual test MOSFETs worked, having similar IV characteristics from what we expected. Light reflection measurements gave us a field oxide thickness of ~500-510 nm, and a gate oxide thickness of 48.2 nm. Electrical testing showed our transistors had a transconductance between 0.42 to 9.8 millisiemens and a threshold voltage of around 0.7V. The circuit itself did not work due to the MOSFETs within our devices not working well and improper connections. This may have been caused by a variety of fabrication issues. The testing of the MOSFETs proved that the circuit theoretically would have worked, but the inconsistency of individual MOSFETs within the full circuit as well as bad metal interconnects within our circuits caused the main half adder circuit and additional subcircuits to fail.

I. INTRODUCTION

The metal oxide semiconductor field effect transistor or MOSFET is one of the most important building blocks in modern day integrated circuits. [12] Using MOSFETs, one can create many different types of circuits including digital logic circuits and analog amplifier circuits. In this work, we will be discussing the design and electrical characterization of the half adder circuit, a digital circuit that is capable of doing basic addition, adding two bits together. In designing the half adder circuit for this lab, we decided to use a design that was completely made out of NAND gates, as this would eliminate the uncertainty in the circuit design and would allow us to more easily split the circuit into different subcircuits, including the NAND gate and the XOR gate. The design of each of the circuits is described as such. The NAND gate is a commonly used logic gate and has a very simple design consisting of a resistor or a load MOSFET and two "choice" MOSFETs arranged in series with each other so that the circuit only turns "on" or has a current flow only when both MOSFETs are on. The NAND gate design that we decided to use had a MOSFET for a load instead of a resistor as in simulation we found that the circuit worked better in SPICE simulation when compared to using a reasonably large resistor. The schematic for the NAND gate used in our half adder circuit is shown in the figure to the right.

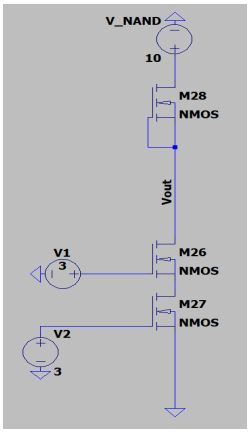
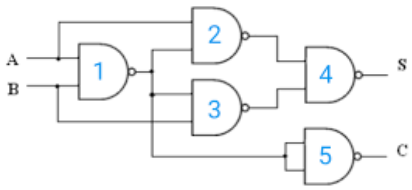


Figure 1. NAND Gate Transistor Level Design

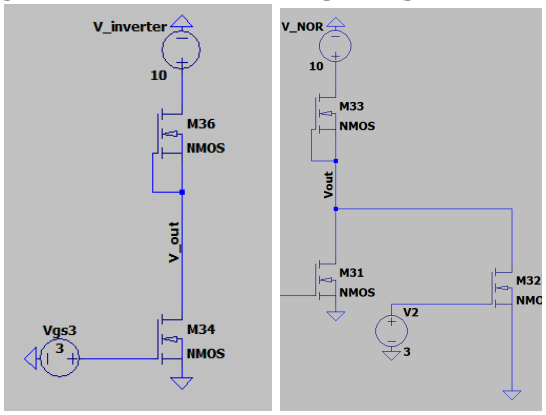
Using the NAND gates, one can use the configuration shown in the figure below to create a half adder circuit.

Figure 2. NAND Gate Digital Gate Level Design



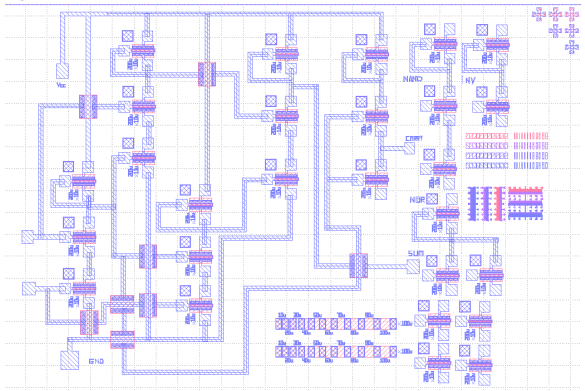
Along with the half-adder circuit design, we also decided to add several sub-circuits to test the circuit in stages and in order to test if a simpler logic gate would work if the full half-adder circuit didn't work as well. The sub-circuits that we added were the previously mentioned NAND gates, the NOR gate and the inverter/NOT gate. The design of each of these gates is very similar to the design of the NAND gate, where we have one or two MOSFETs controlling the current and thus the output voltage for the gates. The design for each of these circuits is shown below.

Figure 3: designs of the Inverter and NOR gates: Inverter left, NOR gate right



After finalizing the circuit design for the half adder and the different sub-circuits, we had to design the 4 masks and fabricate the circuit. The mask itself had a very similar design to the 4 masks used in MOSFET fabrication. The mask itself was designed through the use of Klayout with each of the 4 layers representing the source and drain, gate, diffusion, and metallization layers which are the 4 layers used for MOSFET fabrication. The similarity is to be expected as our circuits only used MOSFETs with no other discrete components needed for our half adder circuit. The final mask design that we created is shown in the following figure. Another point of our design was that the transistors we used for the half adder design were the 200u x 10u transistors. We decided to use these MOSFETs as the measurements that we found in the 120A lab for this specific transistor was the most similar to the transistor model we found in the LTSpice simulator.

Figure 4. Final K-Layout Design of 1 die with all 4 mask layers overlaid on each other

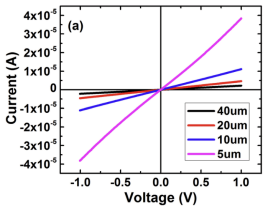
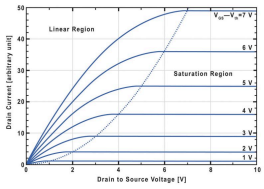
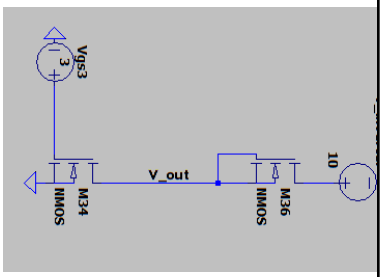
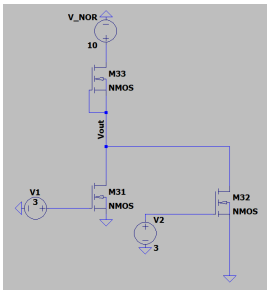
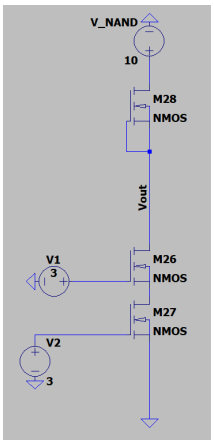
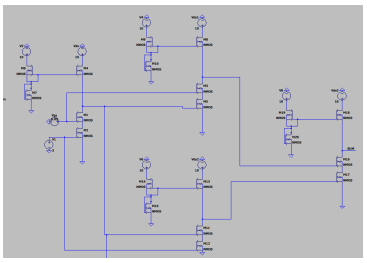
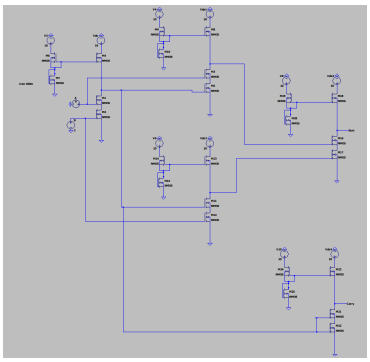


The fabrication process used to physically create the circuit is the same 4-mask fabrication process used to create MOSFETs in the ECE120A lab course. The fabrication process is a complex process requiring the careful execution of many processes, each of which presents its own unique challenges and complications. While in the modern day, sophisticated processes, precise machinery and modern day advancements in materials engineering allow companies to create nanoscale FET devices with very little human input, understanding the process of creating a FET still gives us valuable insights into modern day device fabrication and the considerations needed to be made for IC design and fabrication. [9] The fabrication process used in the lab, as mentioned above, incorporated thermal oxidation, dopant diffusion, photolithography, and an aluminium metallization process. The specific steps as well as any difficulties encountered by our group, will be described in the methodology section of this work. One of the main advantages of the process used in the lab, is that it allows one to fabricate multiple different types of devices and circuits at the same time, on the same sample. The same process used to fabricate our half adder also created a NAND gate, a NOR gate, a NOT gate, test MOSFETs and TLM test pads, which, aside from being important circuits on their own also allow us to test things outside of our entire

circuit and see any potential mistakes made during the fabrication process. [8]

As mentioned above, the fabrication process created the half adder along with a variety of smaller sub circuits, each of them with different electrical characteristics. We will begin the analysis by first describing the tests that we performed to test the circuit and the expected results from each of these electrical tests. For each of the MOSFETs, we performed an Ids versus Vds electrical test while stepping Vgs. For each of the sub-circuits, we performed electrical testing by inputting DC inputs and measuring the DC output to see if we measure a high or low voltage and thus whether or not the circuit works. The expected results as well as a schematic for each test is shown in the table below.

Table 1. MOSFET Expected Results and Digital Circuit Schematics

Test and Schematic	Expected Results
IV Test of TLM pad	 [2]
I_{DS}-V_{GS} MOSFET	 [3]
Inverter	
NOR Gate	
NAND Gate	
XOR Gate	
Half-Adder Circuit	

Shown below are also our expected truth tables and output for each of the sub-circuits and the main circuit of our chip design.

A. Inverter Gate

Table 2. Inverter Truth Table

V1	Expected Value
Logic 0	Logic 1
Logic 1	Logic 0

Figure 5a-b. LTspice Output for a Simple Inverter for high and low inputs

B. NOR Gate

Table 3. NOR Gate Truth Table

(V1, V2)	Expected Value
(0, 0)	Logic 1
(0, 1)	Logic 0
(1, 0)	Logic 0
(1, 1)	Logic 0

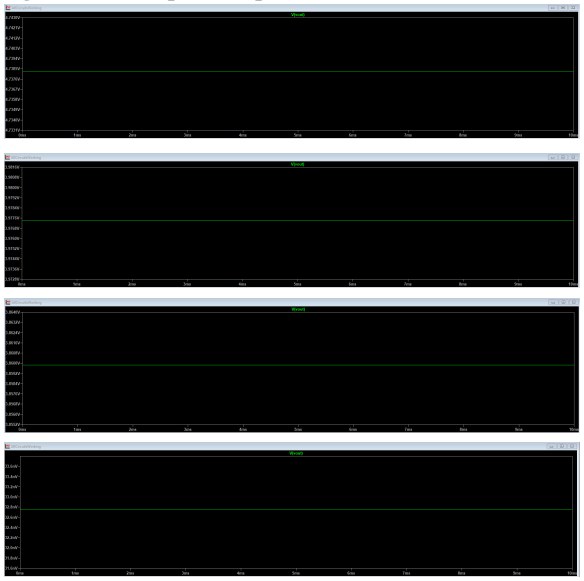
Figure 6a-d. LTspice Output for a NOR Gate

C. NAND Gate

Table 3. NAND Gate Truth Table

(V1, V2)	Expected Value
(0, 0)	Logic 1
(0, 1)	Logic 1
(1, 0)	Logic 1
(1, 1)	Logic 0

Figure 7a-d. LTspice Output for a NAND Gate

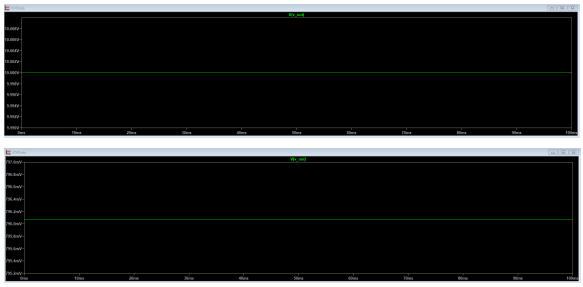


D. XOR Gate

Table 4. XOR Gate Truth Table

(A, B)	Expected Value
(0, 0)	Logic 0
(0, 1)	Logic 1
(1, 0)	Logic 1
(1, 1)	Logic 0

Figure 8a-d. LTspice Output for XOR Gate



E. Half Adder

Table 5. Half Adder Truth Table

Inputs (A, B)	Outputs (Sum, Carry)
(0, 0)	(0, 0)
(0, 1)	(1, 0)
(1, 0)	(1, 0)
(1, 1)	(0, 1)

Figure 9a-d. LTspice Output for NAND-based Half Adder

II.METHODOLOGY

A. Initial Sample Setup and Prep-Work

In the fabrication process, the first step was to cleave samples about 1.5 inch x 1.5 inch in diameter of p-type <100> oriented silicon from a large wafer. We cleaved 4 samples. Of these samples, we had to measure the thickness of the wafer, sheet resistance, and sheet resistivity, estimate carrier concentration and carrier mobility. (shown later)

Next, we had to prep our samples for oxide growth. The process begins with an acetone, 2-propanol, and water cleansing of the samples, followed by a dehydration bake to remove moisture. (solvent cleaning) We then did a standard RCA clean, which involves using an ammonia peroxide solution to remove organic solvents and a HCl solution cleaning step to remove metallic contaminants. This is a change from the ECE 120A lab course, where we only had a piranha clean to remove organic solvents from our chips. This was followed by a quick 10 second dip in buffered hydrofluoric acid (BHF). From here we did a field-oxide growth which used the dry-wet-dry oxide growth procedure to grow 500 nm or 5000 Angstroms of field oxide.

From here, the first measurement we took was to verify that the initial oxide growth had been done properly. We did this using the reflectance box to estimate a rough value and using the Filmetrics' SiO_2 thickness measurement tool to verify that the oxide layer was about 5000A. The reflectance box uses the concept of thin-film interference to show us oxidation colors at different oxide thicknesses and thus gives us an estimate of how thick the layer of oxide grown was. This initial guess is then fed into the filmetrics machine, to give us an accurate reading of the thickness of our chip's oxide growth by shining a light on top of the sample which causes some of the light to reflect off the top surface and others to reflect off underlying layers. The interference pattern created is then fed to a spectrometer which measures the interference pattern and uses it to measure the height of oxide grown on our sample. Through this technique, it non-destructively calculates the thickness of the grown oxide layer. [12]

Next, we measured the thickness of the original wafer, the sheet resistance of the original wafers, and the sheet resistivity with silicon dioxide grown on it. This was done using the 4 point resistivity probe. [13] This machine works by having 2 points applying a current across and 2 points measuring the voltage across. The known resistances of the probes allows the machines to measure the resistance of the sample using Ohm's Law. [1]

Figure 10. Four Point Probe Schematic

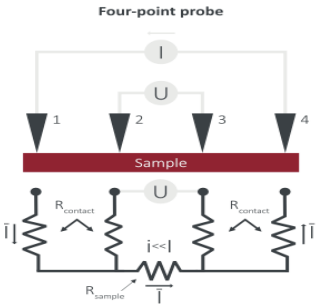


Table 6. Initial Oxide Growth Verification (Angstroms)

#	Q1	Q2	Q3	Q4	Avg
Cont.	-	-	-	-	5050
1	4952.8	4922.9	4931.3	4950	4939.25
2	4991	5002.5	4987.3	4991.5	4993.075
3	5012.6	5052.6	5002.6	5002.9	5017.675
4	4996.8	4998.1	4982.6	4990	4991.875

In our initial growth, our goal was to have 5000A or 500 nm of initial oxide. We see that we ended up growing a little bit more but this should have had minimal effect on the ultimate operation of the FETs. From resistivity measurements, we found that the sample was oxidized properly as the resistance of our sample was measured to be very high. We also know that the carrier type is holes because we were given p-type silicon and can safely estimate that the carrier concentration, N_A. ~= 10^{15} cm^{-3}.

Table 7. Oxide 4 Point Probe Measurements

Sample #	Resistance (Ohms)	Resistivity (Ohms * Thickness)
Control	88.4 Ω	0.0237 Ω*mm
1	>= 9.99 kΩ	At least 4.90 Ω*mm
2	>= 9.99 kΩ	At least 4.93 Ω*mm
3	>= 9.99 kΩ	At least 4.91 Ω*mm
4	>= 9.99 kΩ	At least 4.92 Ω*mm

B. Photolithography and Mask 1 Placement

The first photolithography step involves patterning windows in the field oxide using mask 1 to define areas for n-type dopant diffusion. The process begins with an acetone, 2-propanol, and water cleansing of the samples, followed by a dehydration bake to remove moisture. A layer of hexamethyldisilazane (HMDS) is vapor-deposited to improve adhesion, and AZ 4110 photoresist is spin-coated onto the wafer. After soft baking, a solvent clean of the created mask was done. This is the same process as doing a solvent clean on our chips, except there is no boat and we used a much larger clip to hold the mask in the solvents. Also we do not dehydration bake; we use the N_2 gun to dry off our mask. The resist is exposed using mask layer 1 and developed in AZ 400K developer to reveal the desired pattern. The developed pattern is inspected under a microscope, followed by a hard bake to enhance adhesion and thermal stability. Finally, after taking some microscope pictures to verify proper development, an oxygen plasma descum is performed to remove residual photoresist. This step is crucial as it precisely defines regions where n-type dopants will be introduced, ensuring accurate transistor operation and maintaining the integrity of the device structure. Then, more microscope images were taken and a profilometer reading of the PR thickness was taken. Shown below is the data:

Table 8. PR Height

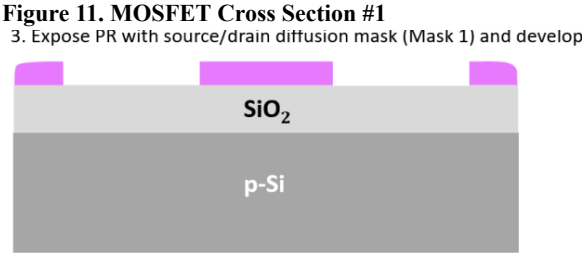
Sample #	Δ Height (μm)
1	1.171
2	1.208
3	1.114
4	1.072

C. Oxide Etching for Diffusion

Note in the previous step we have hard-baked and descumed the photoresist when performing photolithography of mask 1. This is done to prepare for etching as the selectivity of HF, our etchent, targets silicon oxide much more effectively than photoresist so the photoresist

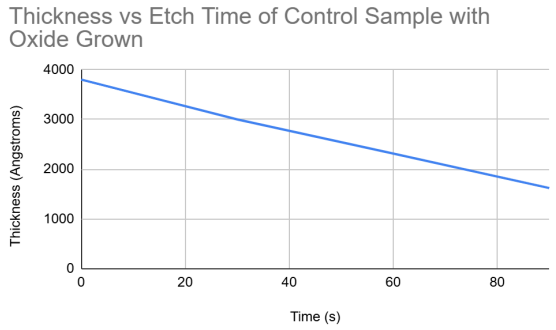
acts as a protective blanket leaving only the silicon oxide to be removed.

Figure 11. MOSFET Cross Section #1



Now we need to etch away the silicon oxide by dipping our sample into hydrofluoric acid. In order to accurately calculate the rate at which the material will dissolve we first must put a control oxidized sample in the HF for a few seconds at a time and measure the remaining oxide to calculate the rate of dissolution, nominally ~100 nm/minute. We measure the oxidation thickness using the filmetrics reflectometer. Overall it's recommended we slightly over etch our sample as underetching means the contacts will remain electrically insulated due to thin layers of oxide that were not fully removed. Due to this we added 20% to our calculated time of 3 minutes and 36 seconds, which ends up being 4 minutes and 19 seconds. See table below for etch rate calculation. The etch rate, slope of this data, would result in 114.3 nm/min.

Figure 12. Etch Rate #1



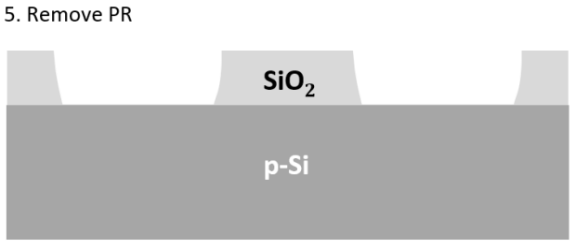
Then we captured microscope images and collected profilometer data:

Table 9. PR and Oxide Height

Sample #	Δ Height (μm)
1	1.67
2	1.707
3	1.621
4	1.576

We then removed the photoresist by dissolving it in acetone and continuing the cleansing cycle with isopropyl alcohol, water and a dehydration bake to get our chips to resemble Figure 6:

Figure 13. MOSFET Cross Section #2



Then we captured microscope images and collected profilometer data seen below. It's important to note that we compared this data to that of our initial oxide measurements to ensure all the oxide was removed before we can continue.

Table 10. Well Depth

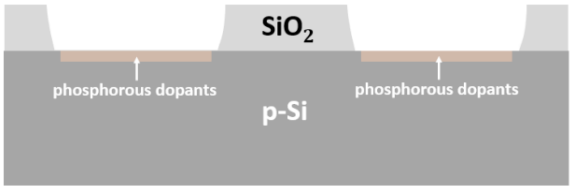
Sample #	Δ Height (μm)
1	0.473
2	0.483
3	0.489
4	0.483

D. Diffusion of n-type Dopant

Now that there's a precise window into the silicon sample it's ready to be doped. First the samples must be thoroughly cleaned at the RCA cleaning bench then in HF for 10 seconds to ensure no other contaminants enter the diffusion furnace. They will undergo 950℃ for 20 minutes so that phosphorus atoms can be blasted and absorbed by our sample. Thanks to the earlier steps, only the silicon exposed by the windows will be doped creating our precisely doped wells. See Figure 7. It should be noted too that this process leaves the samples coated in a layer of phosphorus glass that needs to be removed with another HF dip for 10 seconds.

Figure 14. MOSFET Cross Section #3

7. HF etch to remove phosphorous glass



By measuring our test sample, which was in the same batch as our other samples, we found the inner and outer resistances, resistivity and carrier concentration with an oxide thickness of 525um assuming a mobility of 600 cm^2 per volt second.

$$\rho = R * thickness$$

$$N_d = \frac{1}{q\mu\rho}$$

Table 11. Diffusion Data

	R (Ω)	ρ (Ω/cm)	N_d
Inner	17.8	0.8989	1.32 * 10^-13
Outer	21.8	1.101	1.08 * 10^13

After this n-type dopant diffusion, it is important to not that this is a semiconductor chip, likely with more n-type carriers, so electrons, than p-type.

E. Drive-In Oxide Growth

Drive-in diffusion is needed to achieve a good junction depth which will affect various electrical properties of the FET. It's achieved by growing a layer of oxide over our wells to increase their penetration into the silicon.

To start, our samples need to be cleaned again in preparation for entering a furnace. This means a similar cleaning cycle of acetone, isopropyl alcohol and water. Then it needs to be cleaned of organics and inorganic metals with an RCA clean followed by a 10 second dip in HF to get rid of any other contaminants.

After being inserted to the funrace the sample goes through a dry wet dry oxidation process which just aims at growing high quality oxidized layers. The goal was to grow 300 - 350 nm of oxide so we plugged in these variables into the BYU Growth Calculator and got the time that we needed to leave our samples in. [10 & 14] We grew dry oxide for 10 min, wet oxide for 41 min, and then dry oxide for 10 minutes per our results. Shown below is a cross section of what we've effectively done as well as our oxide growth thickness measurements:

Figure 15. MOSFET Cross Section #4

8. Drive-in diffusion

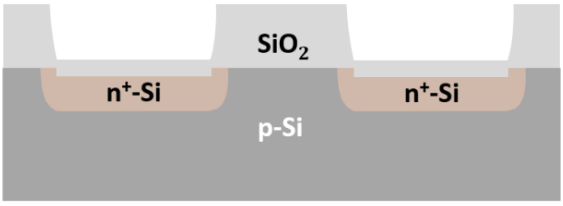


Table 12.Oxide Growth (all measurements in Angstroms):

#	Q1	Q2	Q3	Q4	Avg
1	5200	5458.9	5401.8	5407.6	5367.075
2	5447.1	5454	5453.2	5523.6	5469.475
3	5429.1	5359.2	5425.2	5341.8	5388.825
4	5422.2	5353	5397.2	5366.2	5384.65

F. Photolithography and Mask 2 Alignment

The second photolithography step involves patterning windows in the field oxide using mask 2 to define areas for a thin gate oxide layer. The process follows the same pre-photolithography cleaning and preparation steps as before up to the mask exposure, including cleaning the mask with solvents again in the event that any dust has accumulated while in the case.. Now that there is a pre-existing mask on our sample we have to align this new mask's feature to the existing one using certain markers like the crosses, corner squares, and edges:

Figure 9. Alignment Marker (above)

This process takes a few more minutes but after satisfactory alignment we can continue as usual. We developed in AZ 400K, hard baked, descumed and took data to make sure the thickness looked correct. Our data was taken over the border wells and only serves to check the depth of our features. Shown below is the data:

Table 13. PR Height

Sample #	Δ Height (μm)

1	0.314
2	1.549
3	1.425
4	1.466

It should be noted that at exactly this step, something went wrong with sample 1 as it is a clear outlier from our other data points. (more on this later) From this point, we continued with samples 2-4 and kept sample 1 as an emergency sample in the event that our chips got lost or broken. Going forward, we will only have lab data for Samples 2-4 and will name them samples 1-3 respectively.

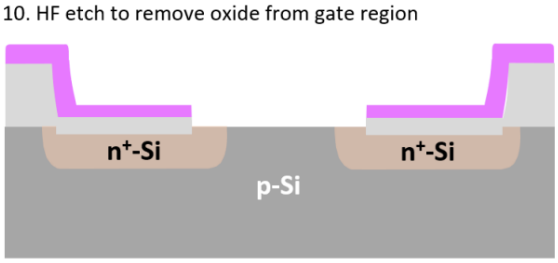
G. Oxide Etching for Growth of Gate Oxide

Note in the previous step we have hard-baked and descumed the photoresist when performing photolithography of mask 2. This is done to prepare for the etching of the silicon oxide block left between the wells and it needs to be etched to install the gate. We assumed similar etch rates as from our mask 1 etching (about 114.3 nm/min). We then took microscope and profilometer data and created a cross section diagram of our FET:

Table 14. PR and Etch Height

Sample #	Δ Height (μm)
1	1.691
2	1.732
3	1.729

Figure 16. MOSFET Cross Section #5



We then removed the photoresist with an acetone cleansing cycle to determine how much we etched away. Then we captured microscope images and collected profilometer data seen below. Again the numbers were very important to make sure we reached silicon and no oxidation remained so that our gate oxide thickness would be more precise.

Table 15. Etch Height

Sample #	Δ Height (μm)
1	0.271
2	0.688
3	0.512

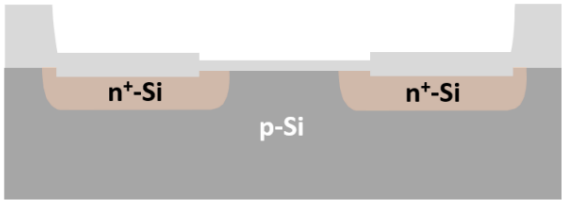
It should be noted that at exactly this step, something went wrong with sample 1 (the original sample 2) as it is an outlier from our other data points. (more on this later) We also considered just focusing our efforts on only sample 2 but we decided to continue on with sample 3 as well. From this point, we continued with samples 3-4 and kept sample 1 and 2 as an emergency sample in the event that our chips got lost or broken. Going forward, we will only have lab data for Samples 3-4 and will name them samples 1-2 respectively.

H. Oxidation Growth of Gate Oxide

We started off this step with a solvent cleansing and dehydration bake, followed up by a comprehensive RCA clean. This was to clean and prepare the samples for dry oxidation. After oxidation, we did a quick 10 second BHF dip to make sure the sample is very clean for oxidation. Next we need to add back in a layer of oxide to make sure our gate is electrically isolated from the body. This step follows a similar procedure as mentioned before except with the goal of growing 40 nm - 50 nm of dry oxide. This amount is much lower than the field oxide growth or dopant growth because a thinner layer of oxide on the gates allows for much better control of the chips when electrical testing. Shown below a schematic of what this would look like:

Figure 17. MOSFET Cross Section #6

11. Remove PR and perform gate oxidation



After using the BYU calculator, we came to the conclusion that we needed to grow oxide for about 42 minutes, using a dry oxidation process. [10 & 14] We started heating up the furnace and working with the lab manager, put our samples into the oxide growth furnace and started a timer. After this growth was complete, we used our control sample and filmetrics to estimate that about 482.3 Angstroms, or 48.2 nm of oxide was actually grown. Shown below is the data for these measurements:

Table 16. Oxide Growth

Sample #	Oxide Growth (Angstroms)
1	482
2	482

I. Photolithography and Mask 3 Alignment

The third photolithography step involves patterning source and drain vias using mask 3. This process follows the same steps as mentioned for both the mask and chips, as mask 2. The goal of this step is again to create a guide for the subsequent etching step to be focused on clearing the oxide for our source and drain vias. Shown below is the data:

Table 17. PR Height

Sample #	Δ Height (μm)
1	1.859
2	1.691

J. Oxide Etching of Sources and Drains

The oxide etching step is crucial for creating contact windows in the oxide layer, allowing metal connections to reach the underlying silicon in the source, drain, and body-bias regions. The process again begins by carefully calibrating the etch rate using buffered HF (BHF) on a test sample. Once the etch rate is determined, all samples are etched for a duration slightly longer than the calculated minimum time to ensure complete oxide removal. Special attention is given to the body-bias contacts, where multiple oxidation layers must be fully etched to establish proper electrical contact with the substrate. Knowing that we grew approximately 482 nm of oxide for the drive in diffusion, and that the etch rate of the day was 114.3 nm/min, with a 20% overetch we had to etch for approximately 5 minutes and 4 seconds.

Step heights are measured using the profilometer, and microscope images are taken to verify that device is free of contaminants and appears well developed:

Table 18. PR and Etch Height

Sample #	Δ Height (μm)
1	1.901
2	2.024

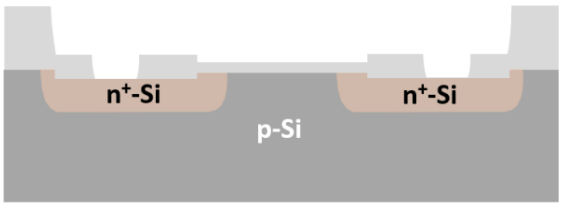
Finally, the photoresist is removed, and additional measurements confirm that the etch depth meets specifications:

Table 19. Etch Height

Sample #	Δ Height (μm)
1	0.681
2	0.678

Figure 18. MOSFET Cross Section #7

14. Remove PR



This step is essential for ensuring reliable electrical connections in the final FET device, as incomplete oxide removal could lead to poor or failed metal contacts, affecting transistor performance.

K. Photolithography and Mask 4 Alignment

The fourth photolithography step involves patterning with mask 4 for metal deposition. The process follows similar steps as

before with a few exceptions. The sample is prepared like usual with an acetone cleaning cycle, HMDS vapor deposition, spin coating and exposure but after that it requires a toluene soak. The toluene softens the photoresist which plays an important role in the metal lift off step. Then the pattern is overdeveloped in AZ 400K developer, without a water rinse as to not tamper with our toluene soak, by about 30-60 additional seconds to reveal the desired pattern. The developed pattern is inspected under a microscope to ensure that the final layer is developed properly. Finally, after taking some microscope pictures to verify proper development, an oxygen plasma descum is performed to remove residual photoresist just as in previous photolithography steps. Again we took profilometer and microscope data. Shown below is the profilometer data:

Table 20. PR Height

Sample #	Δ Height (μm)
1	1.984
2	1.968

L. Metal Evaporation and Lift-Off

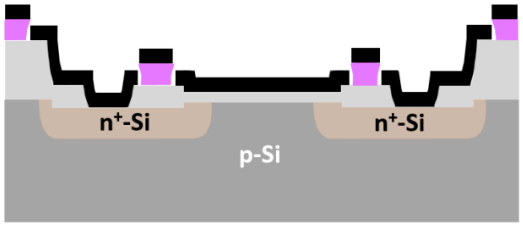
This step started with a quick 10 second HF dip to eliminate any potential oxide remaining on our sample. Then, 300 nm of aluminium metal was deposited onto the samples using the eBeam Physical Vapor Deposition. The instructor did this step for us so we had no difficulties in this step. Then, the samples were submerged in acetone overnight to lift off all unwanted metal. The acetone in this case targets the PR and attempts to dissolve it and thanks to the arrangement of mask 4 they act to discount the even layer of aluminum that coated our sample into the source gate and drain as seen in the figures below. This step would be the final step of the metalization process, essentially eliminating all the excess metal. Fortunately, we were able to get all the metal lifted off to reveal our main die on our chips. We then performed a quick metrology run, capturing microscope imaging and profilometer data:

Table 21. Metal Height

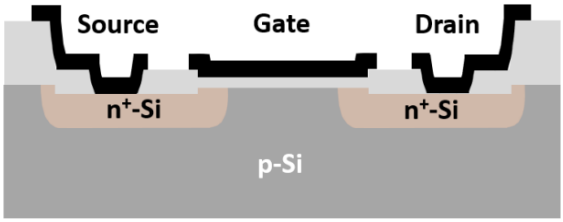
Sample #	Δ Height (μm)
1	0.323
2	0.329

Figure 19-20. MOSFET Cross Section #8-9

16. Evaporate aluminum to form source, drain, and gate electrodes



17. Metal liftoff – Final MOSFET Device!



At this point, we can also analyze the like vernier patterns on the chip to determine how well our masks have lined up. These patterns are like rulers on each of the masks which are all visible on the main die. These rulers should be, in an ideal chip, perfectly aligned. Due to human error while aligning, we have errors in our mask alignment that indicate that our alignment was off by less than a micron for each mask. This is extremely good as our target tolerance we designed for was 5 microns. Shown below are our Vernier Patterns and from this point we transitioned to electrical testing:

Figure 21. Final Alignment Check Sample 1:

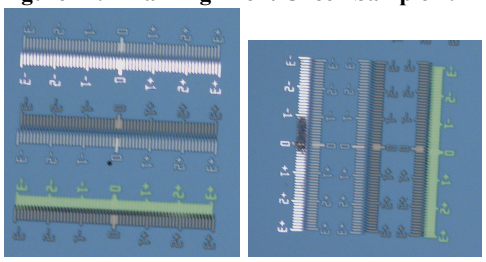
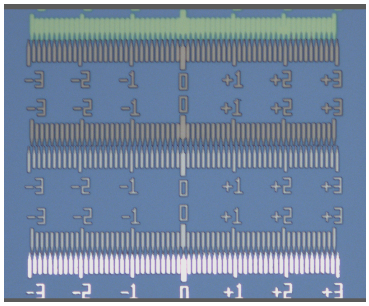


Figure 22. Final Alignment Check Sample 2:



III. RESULTS AND DISCUSSION

A. Electrical Testing Overview

As previously mentioned, we only continued fabrication for sample 3 and 4, so all testing results will be from those samples.

We began by testing our individual devices and test structures followed by some of our subcircuits, and finally our main half adder design. Many of our test structures showed behavior that matched our expectations. Unfortunately, many of our more complicated devices exhibited irregular behavior. In the following sections we will first validate the results of our functional devices by comparing them to theoretical expectations. Then, for our non-functional devices we will analyze their behavior, and propose the most likely fabrication related explanation.

B. Initial Electrical Testing

We began performing electrical testing on our devices. To test for ohmic contacts, we first tested the IV characteristics by performing the two-point test Transfer Length Method on our TLM pads.

Figure 23. TLM Pad I-V Curve 80u

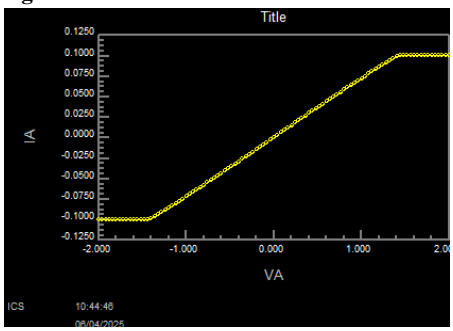


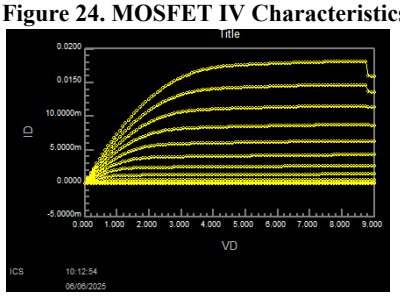
Figure 23 shows the I-V curve for one of our test MOSFETS at a distance of 80um. Our TLMs displayed similar ohmic behavior at other distances as well. From this data, it is clear that all of our TLMs exhibit ohmic behavior. With this in mind we can begin testing our more complex devices.

C. MOSFET Electrical Characterization

We began our electrical testing by testing our FETs. The process to effectively test the IV characteristics of our FETs was a little bit more nuanced than those for our TLM as FETs are 3 terminal devices. This means that if we want to effectively test the $I_{DS} - V_{DS}$ characteristics of our FETs we have to carefully control the voltages we apply to the gate and the drain while maintaining the source at common. For our tests, we stepped the gate voltage from 0V - 5V and swept the drain voltage from 0V - 5V for each of these steps.

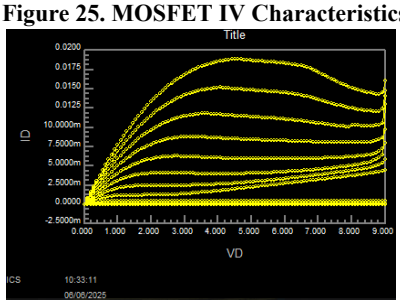
Of the 12 different dies we fabricated, 6 on each chip, we found that at least 75% worked or showed FET IV characteristics, with the rest showing incorrect IV characteristics or nothing at all. [11] Figure 18 shows a good example of what the working FETs' IV characteristics looked like.

Figure 24. MOSFET IV Characteristics



From the MOSFETs without ideal behavior, Figure 19 for example, the IV characteristics are not suitable for accurate testing results of the main circuit, but we continued to test the main circuit and subcircuits for any output, which will be explained in the upcoming sections.

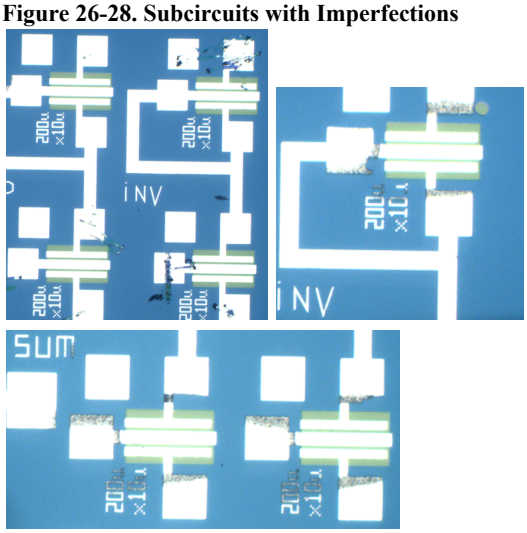
Figure 25. MOSFET IV Characteristics



D. Subcircuit Tests

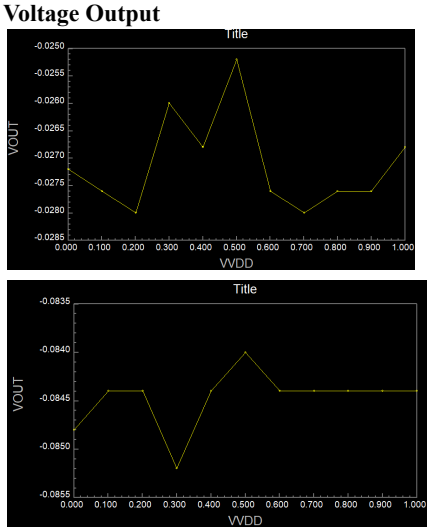
After confirming we have working MOSFETs, we proceeded to test for subcircuit outputs. There is an inverter, NAND, and NOR gate. A few of the circuits have visible imperfections, as shown in Figure 26-28 below.

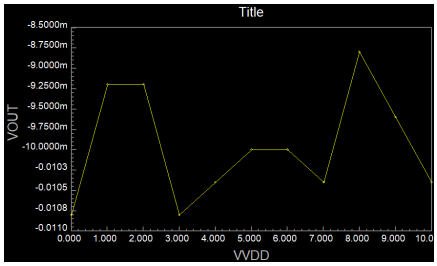
Figure 26-28. Subcircuits with Imperfections



For the procedure of testing the subcircuits, we apply a 0V or 5V voltage signal to the input pads as logic 0 and 1, respectively. Comparing the output graph to a truth table for each gate, we verified that inverter, NAND, and NOR gates do not exhibit an accurate output, shown below.

Figure 29-30. Inverter, NAND Gate, and NOR Gate Voltage Output





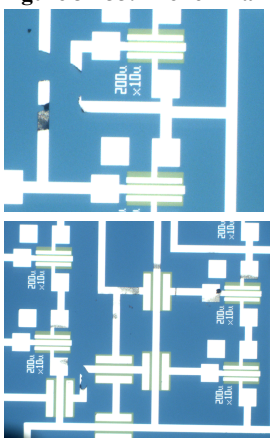
We believe that the imperfections on our circuit are caused by a few reasons. Under the microscope, mask 2 was underdeveloped, showing areas where the features have a gradient, while mask 3 was overdeveloped, making some areas of the circuit blurry and merging electrical contact. Some dark streaks across the sample may also be due to the dust on our samples and mask. Even though we solvent clean the samples and the mask, dust may have gathered from the environment or objects they were in contact with.

E. Main Circuit Test

We had a total of 12 fully fabricated half adder circuits, one on die and 6 die per sample. Unfortunately all 12 of the half adders we fabricated had some type of defect rendering them non-functional. First, we will lay out some of the major defects and common issues that we observed.

One of the most common defects among our half adder circuits was breaks in the actual pathway of the circuitry. In other words, parts of our metal layer were either not deposited properly, or damaged in a way that would not allow electrical signals to pass. One very clear example can be seen in Figure 31 below.

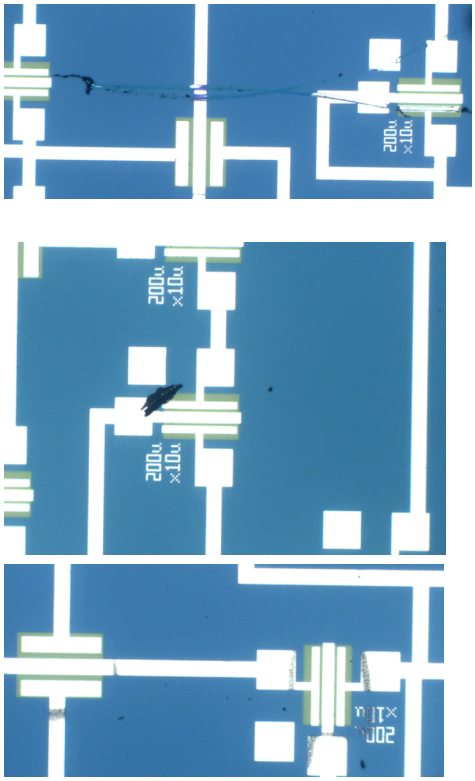
Figure 32-33. Broken Half adder



Clearly our half adders with this type of damage would not work as intended. Despite this, we still wanted an idea of how close we were to producing a working half adder. We were able to find working MOSFETS on 10 out of the 12 adders we fabricated. The two circuits that did not function in any way were next to each other on sample 4, indicating that at some point in the fabrication process, something damaged that section of sample 4.

Our main half adder circuit also had some other defects including some scratches, underdevelopment, and some foreign body artifacts. Examples of these defects from our main adder circuit can be seen below.

Figure 34-36. Scratches, Poor Development, and Artifacts



IV. CONCLUSION

As shown from our results, we were unable to get a working half adder circuit. Although we were not able to successfully produce a half adder circuit on any of our samples this time, the process of designing, fabricating and testing has given us some valuable insights into the semiconductor design process and we were able to create some working MOSFETs that were very similar to the SPICE simulation models which proves that if our MOSFET yield or if the interconnects were better our circuit could have theoretically worked. In this section, we will be breaking down the reasons why our circuit did not work and describe what we could have done better to make the circuit work if we were to redo the process.

We found that most of our single MOSFETs showed reasonably accurate IV characteristics with the transconductance ranging from 0.42 mS to 9.8 mS, a Vth of around 0.7V, and the MOSFET having very little leakage current in our IV plots up to around 7V Vd. These results confirm that our fabrication process was fundamentally correct, as we were able to produce working transistors; however, we were unable to produce a working circuit. When we inspected the samples under the microscope, many of our circuits displayed open or scratched metal connections. While the metal deposition was fine for larger pieces such as the test pads and the TLM pads, which were verified under the microscope and the Vernier patterns verified that our alignment was done properly, we observed inconsistent metal connections and debris or scratches that interrupted some connections within the circuit layouts. This leads us to believe that much of our issues could be solved by having better metal connections in the interconnects or having a cleaner fabrication process.

Another issue that we observed during the fabrication process was the under/over overdevelopment in our masks, specifically mask 2 and mask 3. The issue with the developer was one that had persisted throughout the fabrication process with sample 4 being half over developed and half underdeveloped while sample 3 was slightly under developed for mask 2 and over developed for mask 3 These issues would primarily be due to the developer being very inconsistent throughout the fabrication process with us not being able to find an optimal development time. This issue could be solved with better developers or with more time as that would allow us to strip the PR and start the mask again if needed.

The final issue of note is the fact that the transistor displayed non-ideal activity at a Vds of higher than 7V. This theoretically was fine for our circuit design, but to avoid this, a reasonable change to our design would be to use resistors instead of transistors for the circuit loads. One way that we could potentially test this change is by having the logic gate sub circuits use resistors and have the main circuit use MOSFET loads and see if there is any difference in performance then pick the one that works the best for a final layout/design, though this solution would cost more time and money and would be unviable given the resources and time that we had.

Although the half-adder and our sub-circuits was non-functional after fabrication, this project met its primary goal of educating us about the semiconductor fabrication process. Although we proved that our layout was well thought out by using SPICE simulations with transistor models that were very similar to the MOSFETs produced in the lab, and tested every possible circuit and sub-circuit, we were ultimately unsuccessful in our goal to fabricate a working half adder. Of the many things we can improve on for the future, the most effective solutions would be: focus more on precision during mask alignment to allow for near perfect alignment; tighter development control for all of the masks, and adjust closely post-microscope inspection; possibly more careful cleaning procedures before mask alignment.

AUTHOR CONTRIBUTIONS AND ACKNOWLEDGEMENTS

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