Development and Characterization of N-Type MOSFETs Using a Four-Mask Process

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Abstract - In this work, we will present a comprehensive study of the fabrication and characterization of N-type metal oxide semiconductor field effect transistors, otherwise known as MOSFETs. The four-mask fabrication process used in the lab incorporated thermal oxidation, phosphorus diffusion, photolithography, HF etching, and aluminum metallization and lift off processes to simultaneously create twelve die, each of which includes a variety of devices, including 12 MOSFETs with varying gate width and length sizes, 2 diodes, and a variety of resistors. Light reflection measurements gave us an initial oxide thickness of 490 nm - 492 nm, a gate oxide thickness of 40 nm - 41 nm. Electrical testing characteristics showed our transistors had a transconductance between 0.42 to 9.8 millisiemens. Our diodes had a threshold voltage of about 0.62V and a breakdown voltage of about -38V for our bigger diode, while tests on the smaller diode remained inconclusive. Our capacitance measurements showed expected diode characteristics while the C-V tests for the MOSCAPs and the breakdown voltage for the MOSCAPs were inconclusive.

I. INTRODUCTION

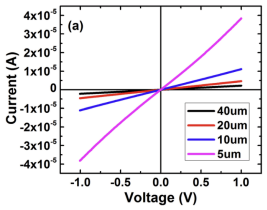
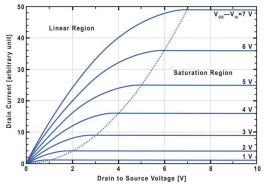
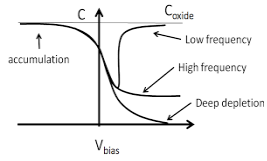
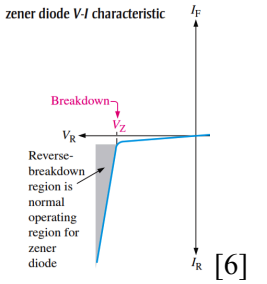
The metal-oxide semiconductor field effect transistor, or MOSFET (FET for short), is one of the most fundamental building blocks of modern-day integrated circuits. [11] The fabrication of FETs is a complex process requiring the careful execution of many processes each of which presents its own unique challenges and complications. While in the modern day, sophisticated processes, precise machinery and modern day advancements in materials engineering allow companies to create nanoscale FET devices, understanding the process of creating a FET still gives us valuable insights into modern day device fabrication. [12] The fabrication process used in the lab, as mentioned before, incorporated thermal oxidation, dopant diffusion, photolithography, and an aluminium metallization process. The steps as well as the difficulties encountered by our group, will be described in the methodology section of this work. One of the main features of the process used in the lab, is that it allows one to fabricate multiple different types of devices at the same time, on the same sample. The same process used to fabricate our N-Type FETs also created several diodes, MOS capacitors, and TLM test resistors, which aside from being important circuit elements on their own, also serve as a test during multiple parts of fabrication and electrical characterization. [10] In this work, we seek to provide an extensive study of a four-mask NMOS fabrication process used during the ECE120A lab. As mentioned above, the fabrication process simultaneously creates a variety of different devices, each of which with its own unique properties that are found through extensive electrical testing. We will first begin our work by explaining the electrical tests and what results we should expect. We will then describe in detail the fabrication processes and the difficulties encountered in each step. Our results will offer valuable insight into the fabrication process.

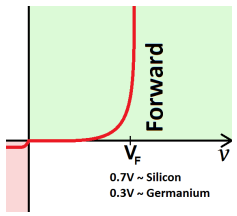
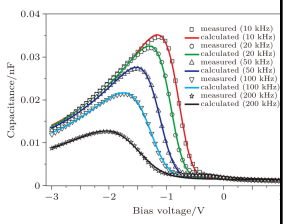
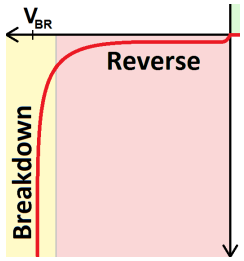
One of the most important aspects of our lab was extensively testing the devices created during the fabrication process. For all devices created, there were multiple current voltage (IV) and capacitance voltage (CV) characteristics which help us test proper device operation. We tested TLM pads, FET characteristics, and diode characteristics.

We performed two probe IV tests on the test TLM pads and the diodes by putting a probe on each end of the device and applying a voltage sweep. After which, performed two probe CV

tests on the diodes and the parasitic gate body and gate source FETs capacitors by running a similar test to our IV tests. We then performed a V_{GS}-I_{DS} three-probe test on the FETs by attaching three probes and applying a voltage sweep on the drain and slowly stepping up the gate voltage. Finally, after collecting all the data we could, we measured the breakdown voltages of the diodes and capacitors by applying a large voltage to the device and performing an IV measurement. The expected results for each test is shown below.

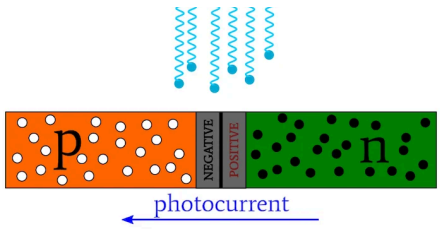
Figure 1. Graphs and Schematics

Test and Schematic	Expected Results
IV Test of TLM pad	 [3]
I_{DS}-V_{GS} MOSFET	 [4]
CV MOSFET & Diode	 [5]
Reverse V_{BR} for MOSFET TEST	 [6]

IV Diodes test	 [7]
CV Diodes	 [8]
Reverse V_{BR} for Diodes	 [7]

When light shines on a semiconductor, incident photons from the light source strike the photodiode and generate electron-hole pairs within the depletion region. This leads to an increase in free charge carriers and in turn a higher conductivity and current across the photodiode when measuring. The source of this light does not matter (microscope light, room light, etc.) as the photons will still strike the surface of the photodiode. These carriers are swept across the P-N junction due to the electric field of the diode, resulting in a photocurrent that adds to the diode's total current in reverse bias. As a general trend, we should find that as illumination intensity increases and more carriers are generated, a larger photocurrent is in turn created. [9] This is shown down below:

Figure 2. Photodiode



This would shift the IV curve downward when the light is on. Similarly, for the CV curve tests, the extra electron-hole pairs impact the depletion width. When light is turned on and illuminates the semiconductor junction, photons with energy greater than or equal to the bandgap energy of the material excite electrons from the valence band to the conduction band, generating electron-hole pairs. These photogenerated carriers significantly alter the electrical properties of the depletion region. These newly generated electron-hole pairs diffuse and drift under the influence of this electric field, effectively reducing the depletion region by increasing conductivity. The increased carrier concentration leads to enhanced recombination and a shift in the equilibrium carrier distribution, which in turn reduces the built-in potential of the junction. This reduction in built-in potential decreases the effective barrier for carrier movement, allowing for an increase in the junction's conductivity. Consequently, the depletion width, which is dictated by the balance of charge within the region, changes dynamically based on the intensity of illumination and the applied bias voltage. A higher light intensity results in a greater density of photogenerated carriers, which further screens the internal electric field and shrinks the depletion width. Since capacitance is inversely proportional to the depletion width, this reduction leads to an increase in junction capacitance. If the photogeneration rate is high enough, it can even lead to complete flattening of the junction potential, significantly altering the CV characteristics and enabling new modes of operation.

II. METHODOLOGY

In the fabrication process, the first three steps which include cleaving and initial field oxide growth, were done for us with us only having to verify the steps had been done properly. The first measurement we took was to ensure that the initial oxide growth had been done properly. We did this using the reflectance box to estimate a rough value and using the filmetrics' SiO_2 thickness measurement tool to verify the oxide layer was about 5000A. The reflectance box uses the concept of thin-film interference to show us oxidation colors at different oxide thicknesses and thus gives us an estimate of how thick the layer of oxide grown was. This initial guess is then fed into the filmetrics machine, to give us an accurate reading of the thickness of our chip's oxide growth by shining a light on top of the sample which causes some of the light to reflect off the top surface and others to reflect off underlying layers. The interference pattern created is then fed to a spectrometer which measures the interference pattern and uses it to measure the height of oxide grown on our sample. Through this technique, it non-destructively calculates the thickness of the grown oxide layer. [1]

Next, we measured the thickness of the original wafer, the sheet resistance of the original wafers, and the sheet resistivity with silicon dioxide grown on it. This was done using the 4 point resistivity probe. This machine works by having 2 points applying a current across and 2 points measuring the voltage across. The known resistances of the probes allows the machines to measure the resistance of the sample using Ohm's Law. [2]

Figure 3. Four Point Probe Schematic

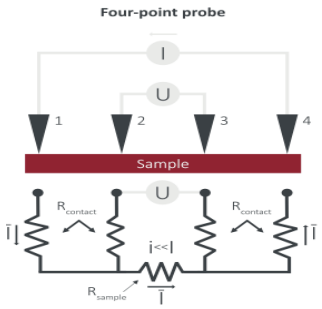


Table 1. Initial Oxide Growth Verification

#	Q1	Q2	Q3	Q4	Avg
Cont.	-	-	-	-	2680
1	4959.1	4927.7	4838.4	4879.8	4901.2

2	4988.9	4941.2	4897.5	4909.1	4934.1
3	4984.6	4937.2	4870.1	4884	4918.9
4	4963.2	4937.5	4862.4	4939.2	4925.5

In our initial growth, our goal was to have 5000A or 500 nm of initial oxide. We see that we ended up growing a little bit less but this should have had minimal effect on the ultimate operation of the FETs. From resistivity measurements, we found that the sample was oxidized properly as the resistance of our sample was measured to be very high. We also know that the carrier type is holes because we were given p-type silicon and can safely estimate that the carrier concentration, N_A. ~= 10^{15} cm^{-3}.

Table 2. Oxide 4 Point Probe Measurements

Sample #	Resistance (Ohms)	Resistivity (Ohms * Thickness)
Control	88.4 Ω	0.0237 Ω*mm
1	>= 9.99 kΩ	At least 4.90 Ω*mm
2	>= 9.99 kΩ	At least 4.93 Ω*mm
3	>= 9.99 kΩ	At least 4.91 Ω*mm
4	>= 9.99 kΩ	At least 4.92 Ω*mm

A. Photolithography and Mask 1 Placement

The first photolithography step involves patterning windows in the field oxide using mask 1 to define areas for n-type dopant diffusion. The process begins with an acetone, 2-propanol, and water cleansing of the samples, followed by a dehydration bake to remove moisture. A layer of hexamethyldisilazane (HMDS) is vapor-deposited to improve adhesion, and AZ 4110 photoresist is spin-coated onto the wafer. After soft baking, the resist is exposed using mask layer 1 and developed in AZ 400K developer to reveal the desired pattern. The developed pattern is inspected under a microscope, followed by a hard bake to enhance adhesion and thermal stability. Finally, after taking some microscope pictures to verify proper development, an oxygen plasma descum is performed to remove residual photoresist. This step is crucial as it precisely defines regions where n-type dopants will be introduced, ensuring accurate transistor operation and maintaining the integrity of the device structure. Then, more microscope images were taken and a profilometer reading of the PR thickness was taken. Shown below is the data:

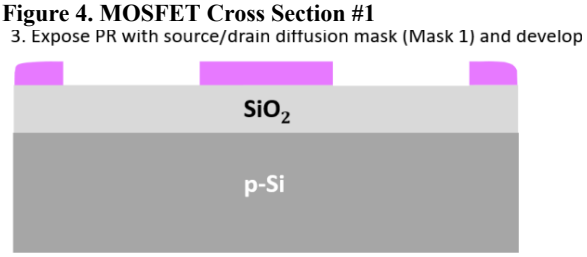
Table 3. PR Height

Sample #	Δ Height (μm)
1	1.121
2	1.098
3	1.069
4	1.084

B. Oxide Etching for Diffusion

Note in the previous step we have hard-baked and descumed the photoresist when performing photolithography of mask 1. This is done to prepare for etching as the selectivity of HF, our etchent, targets silicon oxide much more effectively than photoresist so the photoresist acts as a protective blanket leaving only the silicon oxide to be removed.

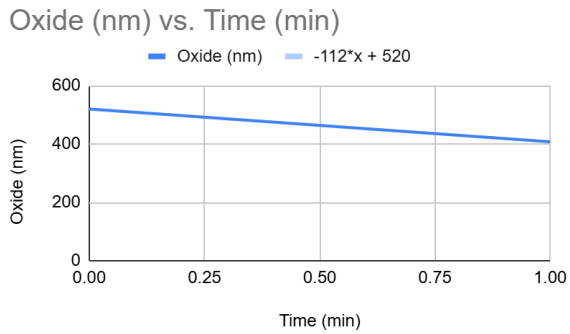
Figure 4. MOSFET Cross Section #1



Now we need to etch away the silicon oxide by dipping our sample into hydrofluoric acid. In order to accurately calculate the rate at which the material will dissolve we first must put a control oxidized sample in the HF for a few seconds at a time and measure the remaining oxide to calculate the rate of dissolution, approximately ~100 nm/minute. We measure the oxidation thickness using the filmetrics reflectometer. Overall it's recommended we slightly over etch our sample

as underetching means the contacts will remain electrically insulated due to thin layers of oxide that were not fully removed. Due to this we added 20% to our calculated time of 4 minutes and 27 seconds, which ends up being 5 minutes and 20 seconds. See table below for etch rate calculation. The etch rate, slope of this data, would result in 118.67 nm/min.

Figure 5. Etch Rate #1



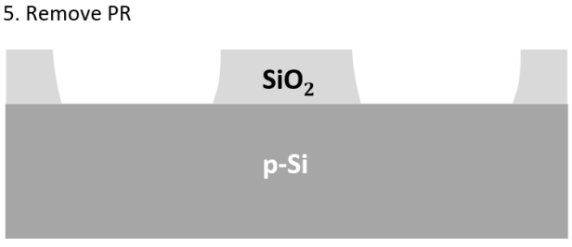
Then we captured microscope images and collected profilometer data:

Table 4. PR and Oxide Height

Sample #	Δ Height (μm)
1	1.703
2	1.641
3	1.575
4	1.604

We then removed the photoresist by dissolving it in acetone and continuing the cleansing cycle with isopropyl alcohol, water and a dehydration bake to get our chips to resemble Figure 6:

Figure 6. MOSFET Cross Section #2



Then we captured microscope images and collected profilometer data seen below. It's important to note that we compared this data to that of our initial oxide measurements to ensure all the oxide was removed before we can continue.

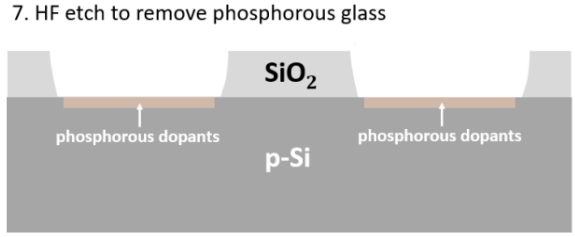
Table 5. Oxide Height

Sample #	Δ Height (μm)
1	0.548
2	0.555
3	0.491
4	0.492

C. Diffusion of n-type Dopant

Now that there's a precise window into the silicon sample it's ready to be doped. First the samples must be thoroughly cleaned in piranha solution for 10 minutes to remove organic contaminants then in HF for 10 seconds to ensure no other contaminants enter the diffusion furnace. They will undergo 950℃ for 20 minutes so that phosphorus atoms can be blasted and absorbed by our sample. Thanks to the earlier steps, only the silicon exposed by the windows will be doped creating our precisely doped wells. See Figure 7. It should be noted too that this process leaves the samples coated in a layer of phosphorus glass that needs to be removed with another HF dip for 10 seconds.

Figure 7. MOSFET Cross Section #3



By measuring our test sample, which was in the same batch as our other samples, we found the inner and outer resistances, resistivity and carrier concentration with an oxide thickness of 525um assuming a mobility of 600 cm^2 per volt second.

$$\rho = R * thickness$$

$$N_d = \frac{1}{q\mu\rho}$$

Table 6. Diffusion Data

	R (Ω)	ρ (Ω/cm)	N_d

Inner	20.4	1.071	9.7*10^15
Outer	22.4	1.176	8.9*10^15

After this n-type dopant diffusion, it is important to not that this is a semiconductor chip, likely with more n-type carriers, so electrons, than p-type.

D. Drive-In Oxide Growth

Drive-in diffusion is needed to achieve a good junction depth which will affect various electrical properties of the FET. It's achieved by growing a layer of oxide over our wells to increase their penetration into the silicon.

To start, our samples need to be cleaned again in preparation for entering a furnace. This means a similar cleaning cycle of acetone, isopropyl alcohol and water. Then it needs to be cleaned of organics with a 10 minute dip in piranha acid followed by a 10 second dip in HF to clean any other materials.

After being inserted to the funrace the sample goes through a dry wet dry oxidation process which just aims at growing high quality oxidized layers. The goal was to grow 300 - 350 nm of oxide so we plugged in these variables into the BYU Growth Calculator and got the time that we needed to leave our samples in. [13 & 14] We grew dry oxide for 10 min, wet oxide for 41 min, and then dry oxide for 10 minutes per our results. Shown below is a cross section of what we've effectively done as well as our oxide growth thickness measurements:

Figure 8. MOSFET Cross Section #4

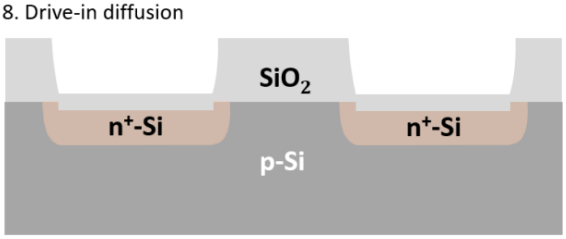


Table 7.Oxide Growth:

Sample #	Oxide Growth (Angstroms)
Control	4249.1
1	5698.4
2	5683.7
3	5543.5
4	5571.7

E. Photolithography and Mask 2 Alignment

The second photolithography step involves patterning windows in the field oxide using mask 2 to define areas for a thin gate oxide layer. The process follows the same pre-photolithography cleaning and preparation steps as before up to the mask exposure. Now that there is a pre-existing mask on our sample we have to align this new mask's feature to the existing one using certain markers like the crosses, corner squares, and edges:

Figure 9. Alignment Marker

This process takes a few more minutes but after satisfactory alignment we can continue as usual. We developed in AZ 400K, hard baked, descumed and took data to make sure the thickness looked correct. Our data was taken over the border wells and only serves to check the depth of our features. Shown below is the data:

Table 8. PR Height

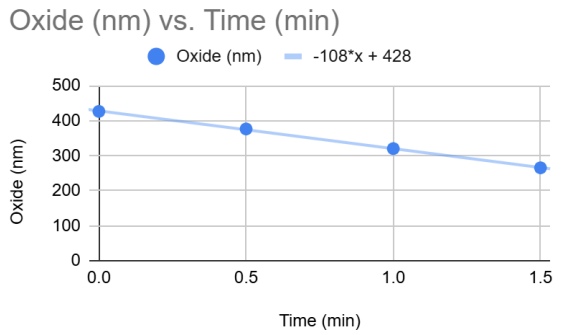
Sample #	Δ Height (μm)
1	1.309
2	1.309
3	1.241
4	1.268

F. Oxide Etching for Growth of Gate Oxide

Note in the previous step we have hard-baked and descumed the photoresist when performing photolithography of mask 2. This is done to prepare for the etching of the silicon oxide block left between the wells and it needs to be etched to install the gate.

Following similar guidelines as stated before, we calculated the etch rate for the day to be 107 nm/min.Knowing we wanted to etch 500 nm and adding 20% for clearance we etched our sample for 5.5 minutes. See our etch rate below:

Figure 10.Etch Rate #2

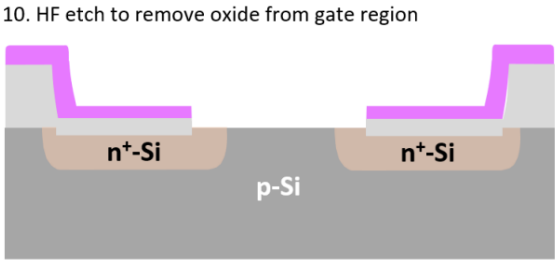


We then took microscope and profilometer data and created a cross section diagram of our FET:

Table 9. PR and Etch Height

Sample #	Δ Height (μm)
1	1.651
2	1.653
3	1.563
4	1.586

Figure 11.MOSFET Cross Section #5



We then removed the photoresist with an acetone cleansing cycle to determine how much we etched away. Then we captured microscope images and collected profilometer data seen below. Again the numbers were very important to make sure we reached silicon and no oxidation remained so that our gate oxide thickness would be more precise.

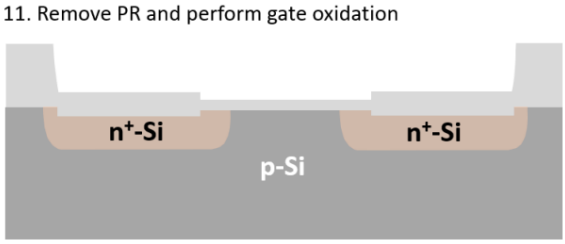
Table 10.Etch Height

Sample #	Δ Height (μm)
1	0.694
2	0.699
3	0.687
4	0.690

G. Oxidation Growth of Gate Oxide

We started off this step with a solvent cleansing and dehydration bake, followed up by a piranha clean for 10 minutes. This was to clean and prepare the samples for dry oxidation. The piranha solution leaves an oxidized layer on top of the chip, which we don't want to interfere with the growth of our oxide in the furnace. Therefore, we did a quick 10 second BHF dip to get rid of this layer of oxidation. Next we need to add back in a layer of oxide to make sure our gate is electrically isolated from the body. This step follows a similar procedure as mentioned before except with the goal of growing 40 nm - 50 nm of dry oxide. This amount is much lower than the field oxide growth or dopant growth because a thinner layer of oxide on the gates allows for much better control of the chips when electrical testing. Shown below a schematic of what this would look like:

Figure 12.MOSFET Cross Section #6



After using the BYU calculator, we came to the conclusion that we needed to grow oxide for about 42 minutes, using a dry oxidation process. [13 & 14] We started heating up the furnace and working with the lab manager, put our samples into the oxide growth furnace and started a timer. After this growth was complete, we used our control sample and filmetrics to estimate that about 400.2 Angstroms, or 40.02 nm of oxide was actually grown. Shown below is the data for these measurements:

Table 11. Oxide Growth

Sample #	Oxide Growth (Angstroms)
1	408
2	411

It should be noted that at exactly this step, we decided to keep samples 3 and 4 as "save points" in case something went wrong in steps 11-14 (which could only be found in step 15). Going forward, we will only have lab data for Samples 1 and 2.

H. Photolithography and Mask 3 Alignment

The third photolithography step involves patterning source and drain vias using mask 3. This process follows the same steps as mentioned for mask 2. The goal of this step is again to create a guide for the subsequent etching step to be focused on clearing the oxide for our source and drain vias. Shown below is the data:

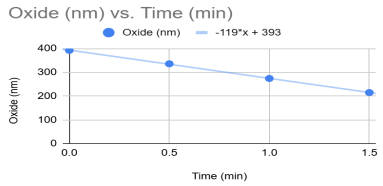
Table 12. PR Height

Sample #	Δ Height (μm)
1	1.652
2	1.647

I. Oxide Etching of Sources and Drains

The oxide etching step is crucial for creating contact windows in the oxide layer, allowing metal connections to reach the underlying silicon in the source, drain, and body-bias regions. The process again begins by carefully calibrating the etch rate using buffered HF (BHF) on a test sample. Once the etch rate is determined, all samples are etched for a duration slightly longer than the calculated minimum time to ensure complete oxide removal. Special attention is given to the body-bias contacts, where multiple oxidation layers must be fully etched to establish proper electrical contact with the substrate. Knowing that we grew approximately 325 nm of oxide for the drive in diffusion, and that the etch rate of the day was 118 nm/min (see data below) we had to etch for approximately 3 minutes and 30 seconds.

Figure 13.Etch Rate #3



Step heights are measured using the profilometer, and microscope images are taken to verify that device is free of contaminants and appears well developed:

Table 13. PR and Etch Height

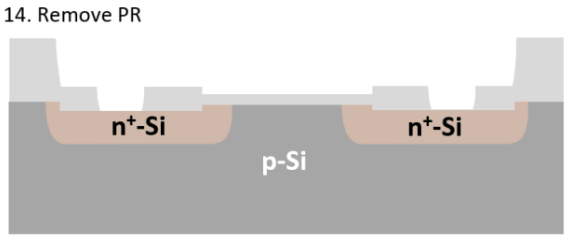
Sample #	Δ Height (μm)
1	1.720
2	1.627

Finally, the photoresist is removed, and additional measurements confirm that the etch depth meets specifications:

Table 14. Etch Height

Sample #	Δ Height (μm)
1	0.678
2	0.623

Figure 14. MOSFET Cross Section #7



This step is essential for ensuring reliable electrical connections in the final FET device, as incomplete oxide removal could lead to poor or failed metal contacts, affecting transistor performance.

J. Photolithography and Mask 4 Alignment

The fourth photolithography step involves patterning with mask 4 for metal deposition. The process follows similar steps as before with a few exceptions. The sample is prepared like usual with an acetone cleaning cycle, HMDS vapor deposition, spin coating and exposure but after that it requires a toluene soak. The toluene softens the photoresist which plays an important role in the metal lift off step. Then the pattern is overdeveloped in AZ 400K developer, without a water rinse as to not tamper with our toluene soak, by about 30-60 additional seconds to reveal the desired pattern. The developed pattern is inspected under a

microscope to ensure that the final layer is developed properly. Finally, after taking some microscope pictures to verify proper development, an oxygen plasma descum is performed to remove residual photoresist just as in previous photolithography steps. Again we took profilometer and microscope data. Shown below is the profilometer data:

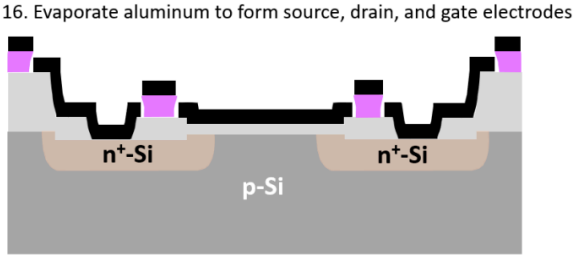
Table 15. PR Height

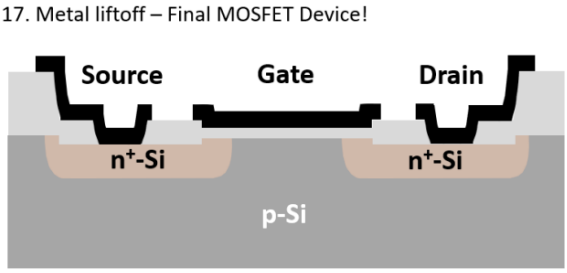
Sample #	Δ Height (μm)
1	1.712
2	1.759

K. Metal Evaporation and Lift-Off

This step started with a quick 10 second HF dip to eliminate any potential oxide remaining on our sample. Then, 300 nm of aluminium metal was deposited onto the samples using the eBeam Physical Vapor Deposition. The instructor did this step for us so we had no difficulties in this step. Then, the samples were submerged in acetone overnight to lift off all unwanted metal. The acetone in this case targets the PR and attempts to dissolve it and thanks to the arrangement of mask 4 they act to discount the even layer of aluminum that coated our sample into the source gate and drain as seen in the figures below. This step would be the final step of the metalization process, essentially eliminating all the excess metal. Fortunately, we were able to get all the metal lifted off to reveal our main die on our chips. We then performed a quick metrology run, capturing microscope imaging and profilometer data:

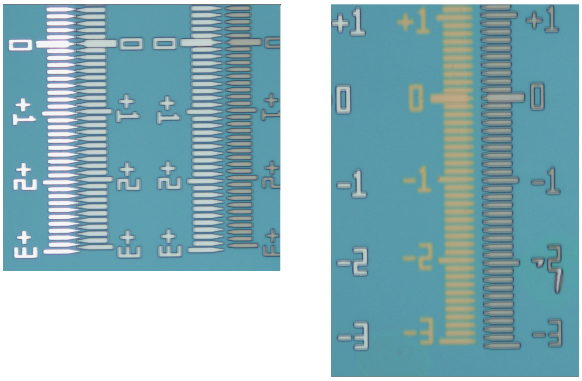
Figure 15-16. MOSFET Cross Section #8-9





At this point, we can also analyze the like vernier patterns on the chip to determine how well our masks have lined up. These patterns are like rulers on each of the masks which are all visible on the main die. These rulers should be, in an ideal chip, perfectly aligned. Given that we naturally produce some sense of human error, we have vernier patterns which indicate all our masks 3 and 4 were off by about 1 micron and our masks 1 and 2 were off by a negligible amount (<< 1 micron) This is extremely good as the thinnest gate of the smallest transistor is 5 microns wide. Shown below are our Vernier Patterns and from this point we transitioned to electrical testing:

Figure 17. Final Alignment Check

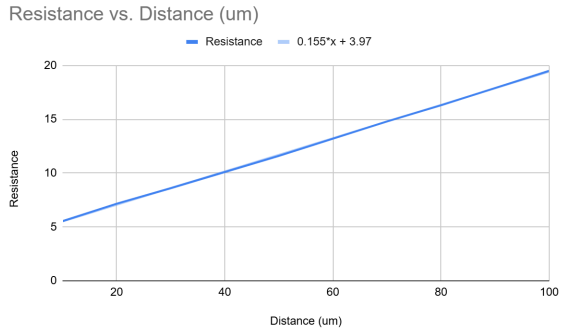


III. RESULTS AND DISCUSSION

A. Initial Electrical Tests

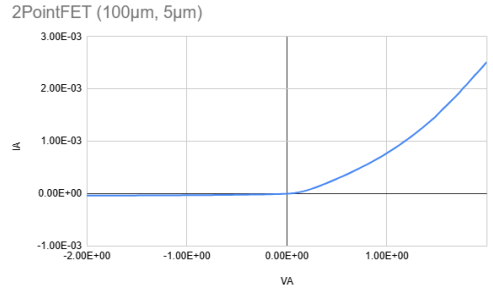
Once we had completed the fabrication process, we began performing electrical testing on our devices. To test for ohmic contacts, we first tested the IV characteristics by performing the two-point test on our drain and source FET contacts. The TLM pre-annealment data is shown in figure 18.

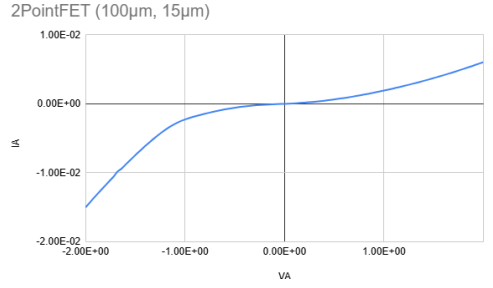
Figure. 18: Slopes of the TLM Data

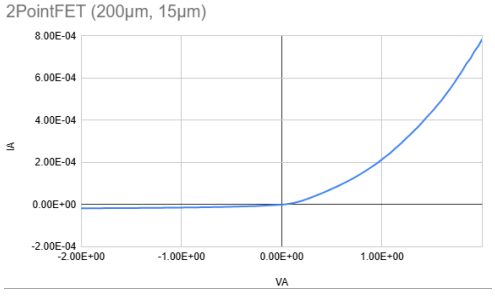


Looking at the data from figure 18, it becomes apparent that all of our TLMs have an ohmic characterization and our sheet resistance is 15.5Ω and contact resistance of 2Ω. The TLM pads showing perfect ohmic behavior lead us to believe that we would not have to anneal as our contacts were already ohmic. As a last check, we also examined some of the drain-source contacts on the FETs using the same two-point probe test. Figures 19a-c display the pre-annealment data for the drain-source FET connection for different drain lengths and gate widths:

Figure. 19a-c: MOSFET Drain/Source Data





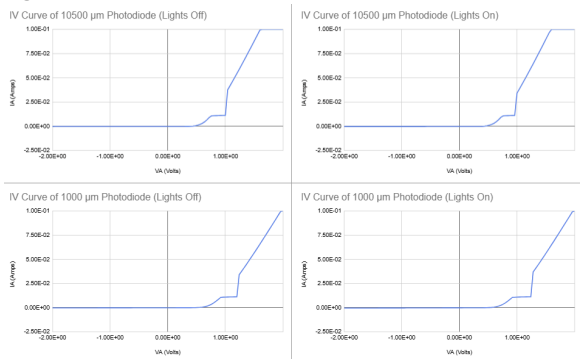


Following these results, we realized that our contacts were not ohmic thus leading us to anneal our samples. The annealing process allows the sample to "repair" itself from ion damage by performing a very controlled diffusion process. After annealment, we found that the V_{GS}-I_{DS} characteristics of our transistors with 2-point probes displayed better behavior than when we tested before the annealment.

B. IV and CV Characteristics of Diodes

After confirming ohmic contact, we measured and plotted the IV and CV characteristics of the diodes produced on the samples. We then compared the results for one of the diodes in the light and dark with the results for our tests shown below.

Figure. 20a-d: Diode IV Curves



From our data, our diodes looked very good with a very evident current jump at a certain voltage through with what seems to be a lower slope than would be normal for a diode. An important note for our data is that there seems to be a small "glitch" in the measurement test bench that occurs around the same spot, right after the V= 0.5V which causes the "dip" seen in our data. This issue persisted through multiple tests and had occurred for multiple other groups. This data isn't a result of our sample but rather is a result of the equipment we used to test and can be ignored.

From our data, we see the expected IV behavior for the diode. To find a good estimation for the turn-on voltage we must draw a tangent line from the point where the curve starts to become exponential. The x-intercept of this curve will be the turn-on, or threshold voltage. Despite minor variations in the four graphs, we estimate that the turn-on voltage, or $V_{T\text{-measured}}$, of the diode is just barely above 0.6V. This is in the

expected range of silicon diodes of 0.6V - 0.7V. [15] The reason why the diode turn on voltage may be slightly lower than expected may be due to differences in the doping levels.

The dark current measured here is the current at a voltage bias far into the negative values (around -2V to -3V) so as to better isolate from any possibility of the diode being excited by external factors. This value must also be measured in the dark. Shown below are the dark currents for the two diodes:

Table 18. Diode Dark Leakage Currents

Diode Length (μm)	Dark Current (Amps)
1000	$-7.72 * 10^{-5}$
10500	$-2.15 * 10^{-4}$

Next we had to measure the series resistance of the diodes. This was done with a simple $R = \Delta V/\Delta I$. While there are more accurate means of measuring this, we have elected to go with this method for its simplicity to repeat measurements and give very good approximations. Much past the turn on voltage (which is now roughly known to be between 0.6 and 0.7 Volts) we can find the slope of any two points. Show below is a table of these series resistances

Table 19. Diode Series Resistances

Diode Length (μm)	Lights State	Series Resistance (Ohms)
1000	On	12.9
1000	Off	12.5
10500	On	17.5
10500	Off	18.3

As we can see, the series resistance seemed to be independent of the state of the light. Finally for the diodes we need to calculate the diode ideality factor. This can be done using the Shockley equation [$n = V/(V_T \ln(I/I_S + 1)]$ where V and I are from our IV curves, and I_S is the saturation current of our device. [19] I_S can be estimated by taking the absolute value of the dark current. Using these the equation, calculated values, and approximations shown above, we have calculated the diode ideality factor, n. This n value range should be around 1-2 for an ideal diode. [16] Below is the table for the calculated diode ideality factor values:

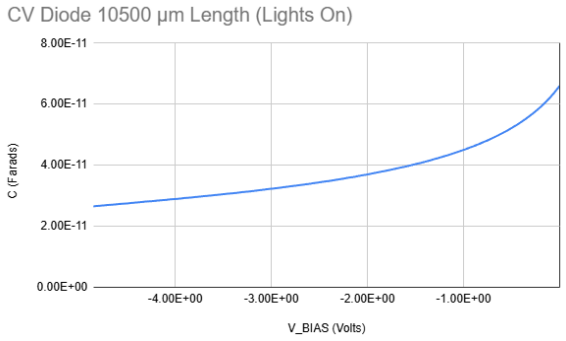
Table 20. Diode Ideality Factor, *n*

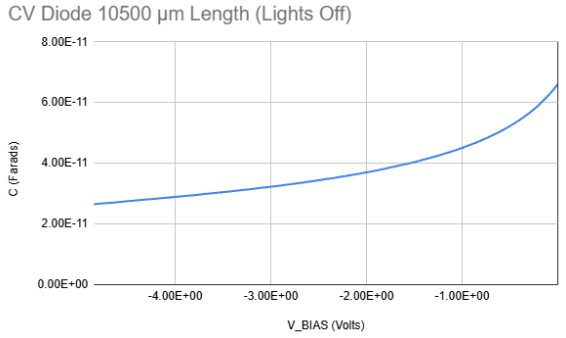
Diode Length (μm)	n-value range
1000	0.43 - 4.65
10500	0.52 - 4.65

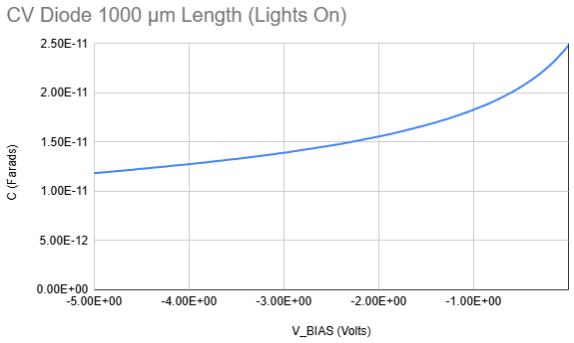
This roughly aligns with the fact that the diode we made, while closer to ideal with sintering, is not an ideal diode as the ideality factor's range is much larger than 1-2. This may be due to contact not being perfectly ohmic which may be caused by misalignment, excess oxidation or a variety of other factors in our fabrication process. It is most likely due to the leakage or dark current measured on our diodes.

After confirming proper IV behavior of our diodes we measured the CV characteristics, the results are shown below**:**

Figure 21a-c: CV Characteristics of Diodes, varying the Length of the Photodiode and the state of the lights







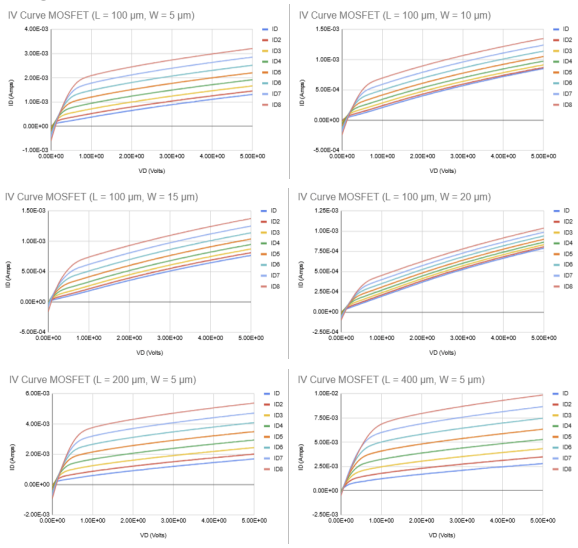
When we took CV measurements for our diodes, we found that as the reverse bias voltage increased, the capacitance decreased. This is an expected behavior for our diode(a P-N junction). In these types of devices, as the bias voltage across them increases, the capacitance decreases. These results indicate that we successfully fabricated working diodes, and similarly, working P-N junctions. Hence, for both the IV and CV characteristics our diodes performed as expected.

C. MOSFET Electrical Characterization

After confirming that our diodes worked properly, we then tested our FETs. The process to effectively test the IV characteristics of our FETs was a little bit more nuanced than those for our TLM or diodes as FETs are 3 terminal devices. This means that if we want to effectively test the $I_{DS} - V_{DS}$ characteristics of our FETs we have to carefully control the voltages we apply to the gate and the drain while maintaining the source at common. For our tests, we stepped the gate voltage from 0V - 0.7V and swept the drain voltage from 0V - 5V for each of these steps.

Of the 12 different FET sizes we fabricated, ranging in gate lengths from 100µm - 400µm and widths of 5µm - 20 µm, we found that 11 out the 12 worked or showed FET IV characteristics with the only one not working being the 400µm x 15µm FET. The results of our tests as depicted in Figures 22a-f effectively show the expected IV relationship discussed in the introduction of this work. As we begin to apply a drain voltage, the drain current increases linearly, until the FETs reach saturation. The saturation point is dependent upon a number of factors such as applied gate voltage and FET width and length. [17] Specifically, an increase in gate voltage or FET width allows for a higher drain current. An increase in FET length will reduce the drain current. Of course, for each of these parameters the converse is also true, ie: a decrease in gate voltage leads to a decrease in drain current. These factors, and parameter relationships detailed above are clearly exhibited by our IV curves tested on each of our various FETs.

Figures. 22a-f: MOSFET IV Curves with varying Drain Lengths and Gate Widths



From our FET IV curves, we can see the effects of gate width and gate length of the FETs. Overall, we found that as the gate width increases the plots of the lines become closer and closer together with all other characteristics remaining the same. As we increase the gate length, we find that the slope of the FET's saturation curve decreases. These observed effects are most likely due to the fact that the FET has more leakage current with a lower gate length or width. This is non-ideal behavior and is most likely due to leakage current on the different capacitors on the FET between gate-source and gate-body. Another observation that we see is that as the gate voltage increases, the saturation point increases. This is an expected behavior of the FET as a higher gate voltage creates a more conductive channel causing it to saturate at a higher voltage. [18]

After finding that our FETs had exhibited the correct I_D-V_D characteristics, we then used the IV characteristic curves to find the transconductance of each fet g_m. To do this we

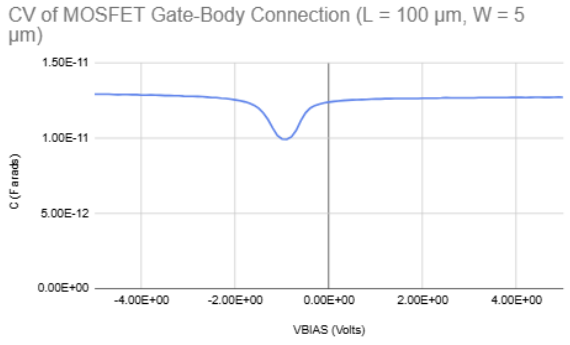
found the change in I_D for each change in V_{GS}. For a more accurate calculation, we would plot many different points on a graph, and the transconductance would be equal to the derivative. Due to the fact that we have a limited number of points, we will be using a discrete delta calculation as opposed to a continuous derivation. The results of our calculations are displayed in table 21.

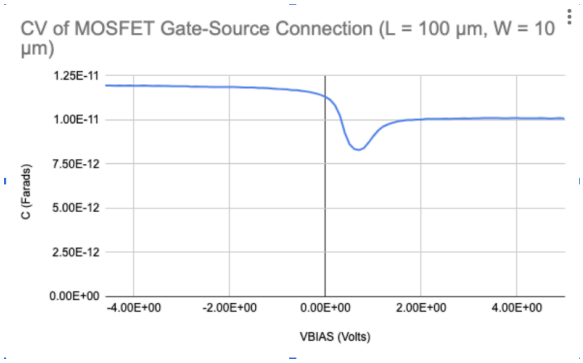
Table 21. MOSFET Transconductance , g_m

MOSFET Length (µm)	MOSFET Width (µm)	$g_m \approx \frac{\Delta I_D}{\Delta V_{GS}}$ (milliSiemens)
100	5	3.33
100	10	1.25
100	15	1.12
100	20	.416
200	5	6.66
400	5	9.8

After measuring the IV characteristics of the FET, we measured the CV characteristics of the gate-source and gate-body capacitors. The results of our CV tests are shown by the graphs. We see that the plots have a dip in the center, signifying the transition from accumulation to depletion and then to inversion. This behavior confirms the behavior of the MOSCAP, where the capacitance stabilizes in strong inversion and reduces in depletion due to the widening depletion region. Similarly, the gate-source capacitance followed the expected trend, where capacitance changes with voltage due to the field effect on the channel region.

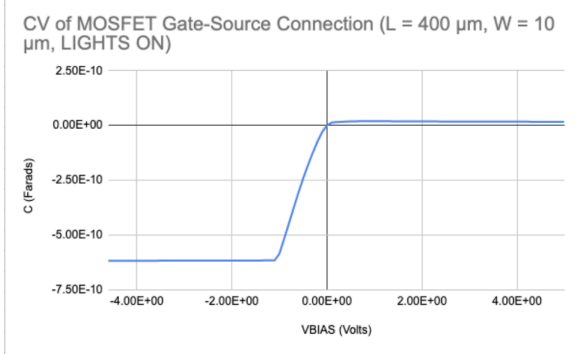
Figures. 23a-b: MOSFET CV Curves for MOSCAPs





We then decided to measure the CV characteristics in the light versus in the dark. These results remained inconclusive as the measured plots for the CV curves, shown in Figure 24, showed very different plots than the data tested previously, shown in figure 23. leading to the possibility that the FET characteristics were not tested properly or that electrical traps or similar imperfections affected the MOSCAPs tested. Based on the data that we were able to collect from our measurements, we saw that there was little change between having the lights on and off. This is an expected result as the CV curves should have had minimal changes since the doping concentration should be much higher than the intrinsic concentration.

Figures. 24a-b: MOSFET CV Curves and changing lights from ON to OFF



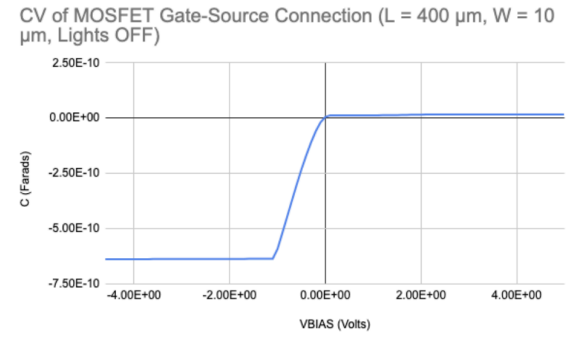
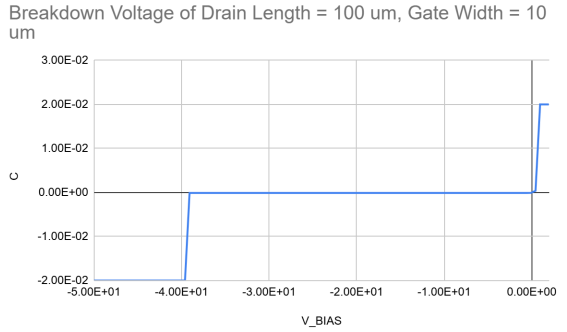


Table 22. Flat-Band Voltages Derived From CV Characterizations

MOSFET Length (μm)	MOSFET Width (μm)	Flat-Band Voltage (V)
100	5	1.8
100	10	0.4
400 (lights on)	10	0.6
400 (lights off)	10	0.5

Figure. 25: MOSFET IV Breakdown



After characterizing our devices to the best of our abilities, we then attempted to measure the breakdown voltages of the MOSCAPs and diodes. Most of these tests were unsuccessful as the MOSCAPs had too much leakage current to be properly measured and the smaller diode was unable to break down even at 100V which was the maximum voltage able to be supplied by the machine. The one breakdown measurement that we were able to get was for the bigger diode which broke down at a voltage of -38V as shown on the IV plot suddenly becoming very negative at this voltage displaying avalanche breakdown. This is to be expected as we heard that other groups had breakdown voltages between 20V - 80V for their diodes. The IV plot used for breakdown also looked like a standard IV characteristic of a diode.

IV. CONCLUSION

This final lab gave us valuable insights into the difficulties and fragility of the process required to create working n-type FETs. To this end, we were able to demonstrate fully functional components through careful electrical testing. Each one of our processes required us to be very precise and careful, where even a small mistake could mean restarting the entire project.

Of the steps, we feel as if the photolithography steps were the hardest and took the most time. Without the use of automation, we had to roughly align using tweezers and steady hands, in addition to checking the mask borders with our raw vision. This was a very difficult and time-consuming process which would have caused operation issues had we misaligned our masks.

The most difficult step was electrical testing. One of the first things we saw was that our TLM graph for voltage and current was linear. This confirms that a metal contact was properly formed during metal lift-off. However, during the testing of the TLM pads, the IV curve was not behaving as we expected. This taught us that sintering was required to improve the metal contact. After sintering, we tested the IV and CV characteristics of the diodes, and they behaved as we expected, apart from the small glitch in the graph caused by the testing gear. Although some of our electrical tests did not work, most likely due to human imperfections, we found that a majority of our measurements properly worked close enough to ideal. Although some of our measurements did not work perfectly or work at all, we most likely could have found a device that worked on one of our die, however this was unable to be accomplished due to the time constraints of this lab. The conclusion that we must draw from this is that although we have discovered a lot, given extra time and more measurements, we would have learned much more. The electrical testing was overall a great test of our patience and a great lesson in learning how to efficiently take measurements.

Fabricating a fully functioning FET was a valuable and rewarding experience. We gained familiarity with a vast array of cleanroom equipment, as well as the entire process of making a FET, similar to major foundries like Intel. This fulfilling project had many key takeaways, with notable ones being patience, precision and control. This was overall a

difficult yet rewarding experience that we were glad to have been a part of.

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REFERENCES

[1] Libretexts, "3: Ideal Diode equation," Engineering LibreTexts, https://eng.libretexts.org/Bookshelves/Materials_Science/Supplemental_Modules_(Materials_Science)/Solar_Basics/D._P-N_Junction_Diodes/3%3A_Ideal_Diode_Equation (accessed Mar. 19, 2025).
[2] Mosfet Physics, https://www.mks.com/n/mosfet-physics (accessed Mar. 19, 2025).
[3] "Ideality factor," Ideality Factor - an overview | ScienceDirect Topics, https://www.sciencedirect.com/topics/engineering/ideality-factor#:~:text=The%20ideality%20factor%20(n)%20is,barrier%20diodes%20have%20n%20%3E%201. (accessed Mar. 19, 2025).
[4] "Ideality factor," Ideality Factor - an overview | ScienceDirect Topics, https://www.sciencedirect.com/topics/engineering/ideality-factor#:~:text=The%20ideality%20factor%20(n)%20is,barrier%20diodes%20have%20n%20%3E%201. (accessed Mar. 19, 2025).
[5] "What is a silicon diode? how does it work?," WaferPro, https://waferpro.com/what-is-a-silicon-diode-how-does-it-work/?srsltid=AfmBOoo292bCuud3rJfHsbD-K-UjYpCm25oFZdoReyi3B6F0xBXjHVyu (accessed Mar. 19, 2025).
[6] "Oxide thickness calculator," Integrated Microfabrication Lab (cleanroom), https://cleanroom.byu.edu/oxidethickcalc (accessed Mar. 19, 2025).
[7] "Oxide growth calculator," Integrated Microfabrication Lab (cleanroom), https://cleanroom.byu.edu/oxidetimecalc (accessed Mar. 19, 2025).
[8] 3NM technology - Taiwan Semiconductor Manufacturing Company Limited, https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm (accessed Mar. 19, 2025).
[9] Author links open overlay panelR.K. Ratnesh a et al., "Advancement and challenges in MOSFET scaling," Materials Science in Semiconductor Processing, https://www.sciencedirect.com/science/article/pii/S1369800121003498 (accessed Mar. 19, 2025).
[10] Contact resistance measurement, https://brightspotautomation.com/wp-content/uploads/2020/05/Contact-resistance-paper-BrightSpot-PVSC2015.pdf (accessed Mar. 19, 2025).
[11] "The physical operation of light-sensitive PN junctions - technical articles," All About Circuits, https://www.allaboutcircuits.com/technical-articles/physical-operation-of-light-sensitive-pn-junctions/ (accessed Mar. 19, 2025).
[12] Modeling capacitance–voltage characteristic of TIW/P-INP Schottky barrier diode, https://cpb.iphy.ac.cn/article/2018/1953/cpb_27_9_097203.html (accessed Mar. 19, 2025).
[13] "Diodes," Diodes - SparkFun Learn, https://learn.sparkfun.com/tutorials/diodes/real-diode-characteristics (accessed Mar. 19, 2025).
[14] Bharadwaj, "Zener diode breakdown characteristics," Engineering Tutorial, https://engineeringtutorial.com/zener-diode-breakdown-characteristics/ (accessed Mar. 19, 2025).
[15] Measured curves and dual-frequency corrected C-V curves for MOS... | download scientific diagram, https://www.researchgate.net/figure/Measured-curves-and-dual-frequency-corrected-C-V-curves-for-MOS-capacitors-with-different_fig4_225580100 (accessed Mar. 19, 2025).
[16] "P-channel MOSFET," MathWorks, https://www.mathworks.com/help/sps/ref/nchannelmosfet.html (accessed Mar. 19, 2025).
[17] TLM of the sidewall ohmic contacts - researchgate, https://www.researchgate.net/figure/TLM-of-the-sidewall-ohmic-contacts_fig8_260319997 (accessed Mar. 19, 2025).
[18] "Four point probe measurement method," SURAGUS Everything about Four Point Probe Measurement, https://www.suragus.com/en/technology/four-point-probe/ (accessed Mar. 19, 2025).
[19] Inc. Filmetrics, "Thickness measurement of indium tin oxide (ito) and other transparent conductive oxides (tcos)," ITO Film Thickness and Transparent Conductive Oxide Thin Film Thickness Measurement, https://www.filmetrics.com/applications/ito#:~:text=The%20Filmetrics%20F20%2DEXR%20film,accurate%20ITO%20film%20thickness%20measurements. (accessed Mar. 19, 2025).